

PCI Express Endpoint Controller

Highlights :

- *Silicon Proven*
- *PCI-SIG Compliant*
- *Complete solution with PCI Express Transaction, Data-link, MAC-PHY and Configuration for end point devices*
- *Extremely low latency*
- *Fully Compliant with PCIE 1.0a and 1.0a Errata and PIPE interface*
- *Up to 8 VCs and 8 TCs*
- *Industry's Lowest RAM instance count solution*
- *Supports all power down states*
- *Supports beaconing, receiver and electrical idle detection*
- *Built with QOS features*

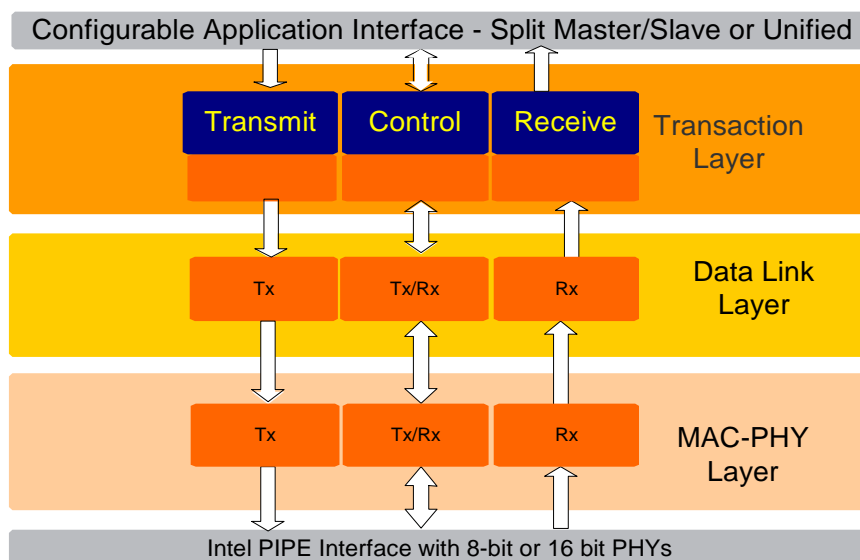
TALLIKA CORPORATION

2222 S. Dobson Rd, Suite 1103
Mesa, AZ 85202

Phone: 480 231 2074

www.tallika.com

Email: sales@tallika.com



Tallika's PCI Express endpoint core is a silicon proven, PCI SIG compliant, flexible and scalable endpoint solution built by experts with years of experience in building PC System Controllers (for Pentium and Alpha microprocessors) as well as multi-gigabit Networking chips. With a rigorous randomized self test environment and a methodology developed while implementing complex system controllers and networking ASICs. Low gate count, buffered memory reads and writes to avoid timing surprises, flexible Tx/Rx RAM configurations, no latches, and physical synthesis friendly design. Low gate count solution will work for both ASICs and FPGAs.

Features:

- ◆ Complete implementation of PCI Express Transaction, Data Link, MAC-PHY and Configuration layers for an Endpoint device.
- ◆ Industry standard PIPE interface for the PHY interface, with support for 8-bit, and 16-bit PHY's—ability to work with any PIPE 1.0 compliant PHY.
- ◆ Easily extensible to support root complex and switch solutions along with crosslink support
- ◆ Unique high performance application interface with support for patent-pending high throughput, low-latency “Pause-and-resume” technology
- ◆ Configurable Transmit/Receive Cut-through mode reduces latency by transmitting before complete packet is received from/to the application side.
- ◆ Ability to accept read request larger than the Max Read Request Size. The core splits single Memory Read request into multiple TLPs and assembles out of order received completions before presenting to the application interface
- ◆ Configurable widths of $x1$, $x2$, $x4$ @ 125 Mhz or 250 MHz, $x8$ @ 250 MHz with 64-bit with down scaling of lane widths
- ◆ Scalable to support widths of $x8$, $x12$, $x16$ @ 250 Mhz with 128-bit datapath with down scaling of widths
- ◆ Supports configurable multiple traffic classes ($TC0-TC7$) on one or more virtual channels ($VC0-VC7$).
- ◆ Configurable number of Maximum TLP commands on TX and RX directions. Supports up-to 32 tagid's as well as support for up to 256 tagid's with extended tag enabled.
- ◆ Separate Initiator and Target interface on application side, configurable to be a shared interface.
- ◆ Ability to configure through a local application configuration interface.
- ◆ Configurable size of data buffers on TX and RX directions. Single merged data and retry buffer on TX direction, and a single buffer for RX direction. Initiator and Target buffers can be configured as separate or merged.
- ◆ User specified ‘UserID’ for commands on master and target provides simple application interface. Core maintains generation of PCI Express tagid's.
- ◆ Ability to accept Pre-formed TLP packets from application for transmission and forwarding of received TLP packets to application.
- ◆ Optional ECRC generation and checking support for TLP
- ◆ Maintains PCI Express Ordering rules based on Relaxed Ordering bit for Initiator and Target transactions.
- ◆ Optional *Advanced Error Reporting* support
- ◆ Manages Flow control in TX and RX directions for Posted, Non-Posted and Split Completion transactions
- ◆ In Physical layer, support for Link initialization and training, LTSSM, Compliance pattern generation, Data Scrambling.
- ◆ Optional Support for Lane Reversal, Polarity inversion.
- ◆ Supports Active State Power Management (ASPM) and Software compatible PCI-PM. Optional Support for D1 and D2 states.
- ◆ Complete message support for INTx, MSI (User Defined Messages), PME
- ◆ Suitable for any technology 0.18u or below .
- ◆ Optional Power Budgeting capability support.
- ◆ Optional Device Serial Number capability

Deliverables:

- ◆ Verilog RTL
- ◆ Testbench and behavioral models with test-cases
- ◆ Primetime and DC scripts—support available for Magma and Cadence design flows
- ◆ Complete documentation with Integration Guide

©2005 Tallika Corporation